Replacement Abstract

A method and apparatus is provided for significantly speeding-up program execution in a data processing device. The data processing device is provided with a specialized instruction region storage section comprising content addressable memory (CAM) and random access memory (RAM) that operatively functions as an instruction sequence reuse table which is capable of registering/storing sequences of program instructions and corresponding instruction sequence output data as input/output (I/O) groups for potential future use in place of re-executing identical portions of program code. The data processing device includes at least one instruction stream processor which includes a computing unit for executing instructions and a dependency relationship analysis unit or "reuse window" unit (RW) that analyzes instruction sequence patterns from regions of instructions stored in a main memory to determine if the patterns can be divided up into smaller partitions that have no interdependencies and hence are potential candidates for reuse.